

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 to 12. (Canceled)

1 13. (Previously Presented) A digital system having a
2 microprocessor operable to execute a rounding dot product
3 instruction, wherein the microprocessor comprises:

4 storage circuitry for holding pairs of elements;

5 a multiply circuit connected to receive a first number of
6 pairs of elements from the storage circuitry in a first execution
7 phase of the microprocessor responsive to the dot product
8 instruction, the multiply circuit comprising a plurality of
9 multipliers equal to the first number of pairs of elements;

10 an adder/subtractor circuit having a plurality of inputs each
11 connected to receive a corresponding one of the plurality of
12 products from the plurality of multipliers and a mid-position carry
13 input to a predetermined bit for mid-position rounding responsive
14 to the rounding dot product instruction; and

15 a shifter connected to receive an output of the
16 adder/subtractor circuit, the shifter operable to shift a selected
17 amount in response to the rounding dot product instructions.

Claims 14 to 24. (Canceled)

1 25. (Previously Presented) A data processing apparatus
2 comprising:

3 a first multiply circuit having first and second inputs and an
4 output, said first multiply circuit operable in response to a dot
5 product instruction to multiply data received at said first and
6 second inputs and generate a first product at said output;

7 a second multiply circuit having first and second inputs and
8 an output, said second multiply circuit operable in response to a
9 dot product instruction to multiply data received at said first and
10 second inputs and generate a second product at said output;

11 an adder/subtractor circuit having first and second inputs, a
12 mid-position carry input to a predetermined bit and an output, said
13 first input receiving said first product from said first multiply
14 circuit, said second input receiving said second product from said
15 second multiply circuits, said adder/subtractor circuit operable in
16 response to said dot product instruction to arithmetically combine
17 said first and second products and a "1" input at said mid-position
18 carry input of said predetermined bit thereby forming a
19 mid-position rounded sum; and

20 a shifter connected to receive said mid-position rounded sum
21 of the adder/subtractor circuit, the shifter operable to shift said
22 mid-position rounded sum a predetermined amount in response to said
23 dot product instruction.

1 26. (Previously Presented) The data processing apparatus of
2 claim 25, wherein:

3 said arithmetic combination of said first and second products
4 is an arithmetic sum.

1 27. (Previously Presented) The data processing apparatus of
2 claim 25, wherein:

3 said dot product instruction is a dot product with negate
4 instruction; and

5 said arithmetic combination of said first and second products
6 is a difference of said second product from said first product in
7 response to said dot product with negate instruction.

1 28. (Currently Amended) The data processing apparatus of

2 claim 25, further comprising:
3 a first Q shifter having an input receiving said first product
4 from said first multiply circuit and an output supplying said first
5 input to said adder/subtractor circuit, said first Q shifter
6 shifting said first product an instruction specified number of bits
7 responsive to the rounding dot product instruction; and
8 a second Q shifter having an input receiving said second
9 product from said second multiply circuit and an output supplying
10 said second input to said adder/subtractor circuit, said second Q
11 shifter shifting said second product said instruction specified
12 number of bits responsive to the rounding dot product instruction.

1 29. (Previously Presented) The data processing apparatus of
2 claim 25, wherein:
3 said first multiply generates said first product in a
4 redundant sign/magnitude format;
5 said second multiply circuit generates said second product in
6 said redundant sign/magnitude format;
7 said adder/subtractor circuit arithmetically combines said
8 first and second products and said "1" input at said mid-position
9 carry input forming said mid-position rounded sum in said redundant
10 sign/magnitude format;
11 a shifter shifts said mid-position rounded sum in said
12 redundant sign/magnitude format; and
13 said data processing apparatus further comprises a carry save
14 adder to 2's complement converter having an input receiving said
15 shifted mid-position rounded sum in said redundant sign/magnitude
16 format and an output generating a corresponding normal coded
17 format.